TEXAS INSTRUMENTS

TPS6205xEVM

Low-Power, DC-DC EVM for High-Efficiency, Step-Down Converters

User's Guide

February 2003

PMP EVMs

SLVU081

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.7 V to 10 V and the output voltage range of 0.7 V and 6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the operation of the TPS6205xEVM low-power, dc-dc evaluation module for high-efficiency, step-down converters.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Evaluation With the TPS6205xEVM
- Chapter 3—PCB Layout

Related Documentation From Texas Instruments

- TPS6205x data sheet (SLVS432)

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Contents

Figures

Tables

Chapter 1

Introduction

The Texas Instruments TPS62050 and TPS62052 evaluation modules (EVM) for low-power, high-efficiency, step-down converters help designers evaluate these devices. The EVMs make it possible to evaluate different modes of the devices as well as the device performance.

The TPS6205xEVM is available as the TPS62050 adjustable version set to 3.3 V and the TPS62052 1.5-V fixed version.

The TPS62050EVM can be easily set up to provide any output voltage between 0.7 V to 6 V (or Vin) by adjusting the external resistor divider. Refer to the data sheet (SLVS432) for various fixed voltage options available for the TPS6205x. The TPS6205x has an input voltage range between 2.7 V and 10 V with an output current up to 800 mA.

Any version of the TPS6205x can be evaluated by removing and replacing the IC on the EVM.

Topic **Page**

1.1 EVM Ordering Information

Table 1–1. EVM Ordering Information

EVM Number	Description
TPS62050EVM–234	Adjustable output voltage version set to 3.3 V
TPS62052EVM–234	1.5-V fixed output voltage version

Chapter 2

Evaluation With the TPS6205xEVM

This chapter details the evaluation process and features of the EVM. For this purpose, a load is connected to the output pins Vout and GND, which allows the load current to be adjusted between 0 mA and 800 mA.

For accurate output voltage and input voltage measurements, it is important to measure the voltage on the input and output voltage terminals with a voltmeter connected directly to the input voltage or output voltage terminals. This eliminates any measurement errors related to voltage drops along the input and output terminal wires connected to the power supply or load.

Topic **Page**

2.1 Enable (EN) Jumper

This jumper is used to enable the device. Connecting the EN pin to ON enables the part. Connecting the EN pin to OFF disables the device.

2.2 Synchronization (SYNC) Jumper

This jumper is used to choose between PWM and PFM/PWM modes of operation. Setting the jumper across PWM forces the device into the low-noise fixed-frequency pulse width modulation (PWM) mode. Setting the jumper across PWM/PFM enables the power save mode where the device enters a pulse frequency modulation mode (PFM) at light to medium load currents, which reduces quiescent current and switching frequency to a minimum to achieve highest efficiency over the entire load current range.

Additionally an external clock between 600 kHz and 1200 kHz can be applied to pin 2 of J2 (SYNC) in order to synchronize the converter to an external clock.

2.3 Power Good (PG)

The PG pin is an open drain output capable of sinking typically 1 mA. A pullup resistor is required to use the PG. The pullup resistor should be placed between the Vout and PG. The PG pin becomes active high when the output voltage exceeds typically 98.5% of its nominal value. Leave the PG pin unconnected when not used.

2.4 Low Battery Out (LBO)

The LBO pin is an open drain output which goes low when the voltage at the low battery input (LBI) falls below the trip point of 1.21 V. An external pullup resistor which is placed between LBO and Vout is required to use the LBO.

Chapter 3

PCB Layout

As for all switch mode power supplies, the PCB layout is a very important step in the power supply design process. The following figures show the layout for the adjustable and fixed output voltage EVMs.

Topic **Page**

3.1 SLVP234 EVM Schematic and Bill of Materials

Figure 3–1 shows the SLVP234 EVM schematic diagram. The bill of materials for the TPS62050EVM and TPS62052EVM is shown in Table 3–1. More details about the design and component selection for the dc-dc converter can be found in the data sheet.

Figure 3–1. TPS62050EVM and TPS62052EVM (SLVP234) Schematic

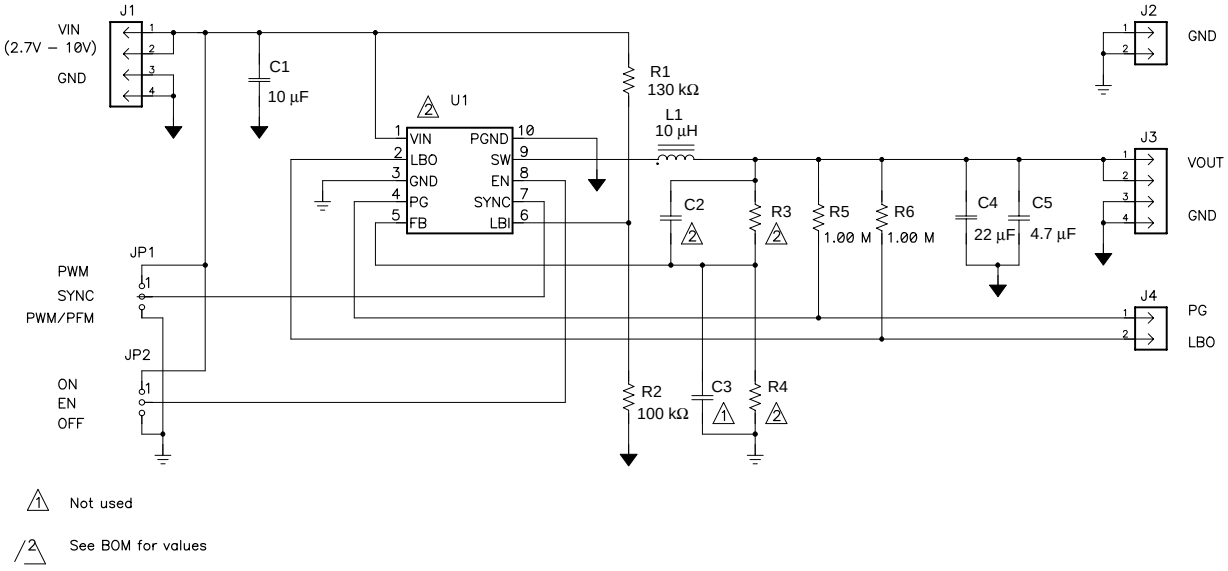

Table 3–1. TPS62050 and TPS62052 EVMs (SLVP234) Bill of Materials

Count		Ref				
TPS62050	TPS62052	Des	Description	Size	MFR	Part Number
1	1	C1	Capacitor, Ceramic, 10 µF, 16 V, X5R, 10%	1210	Murata	GRM32ER61C106KC31
1	open	C2	Capacitor, ceramic, 22 pF, 50 V, C0G, 5%	603	Murata	GRM1885C1H220JZ01
open	open	C3	Capacitor, ceramic, xx µF, xx µV	603		
1	1	C4	Capacitor, ceramic, 22 µF, 6.3–V, X5R, 10%	1210	Murata	GRM32DR60J226KA01
1	1	C5	Capacitor, ceramic, 4.7 µF, 6.3 V, X5R, 10%	805	Murata	GRM219R60J475KE11
2	2	J1, J3	Header, 4 pin, 100 mil spacing, (36-pin strip)	0.12	Sullins	PTC36SAAN
2	2	J2, J4	Header, 2 pin, 100 mil spacing, (36-pin strip)	0.12	Sullins	PTC36SAAN
2	2	JP1, JP2	Jumper, 3 pin, 100 mil spacing, (36-pin strip)	0.12	Sullins	PTC36SAAN
1	1	L1	Inductor, SMT, 10 µH, 1.4 A, 63.6 mΩ	0.276 sq	TDK	SLF7032T–100M1R4
1	1	R1	Resistor, chip, 130 kΩ, 1/16 W, 1%	603	Std	Std
1	1	R2	Resistor, chip, 100 kΩ, 1/16 W, 1%	603	Std	Std
1		R3	Resistor, chip, 562 kΩ, 1/16 W, 1%	603	Std	Std
	1		Resistor, chip, 0 Ω, 1/16 W, 5%	603	Std	Std

Table 3–1. TPS62050 and TPS62052 EVMs (SLVP234) Bill of Material (Continued)

Count		Ref				
TPS62050	TPS62052	Des	Description	Size	MFR	Part Number
1	open	R4	Resistor, chip, 100 kΩ, 1/16 W, 1%	603	Std	Std
1	1	R5	Resistor, chip, 1.00 MΩ, 1/16 W, 1%	603	Std	Std
1	1	R6	Resistor, chip, 1.00 MΩ, 1/16 W, 1%	603	Std	Std
1		U1	IC, high-efficiency step-down converter, Adj V	DGS10	TI	TPS62050DGS
	1		IC, high-efficiency step-down converter, 1.5 V	DGS10	TI	TPS62052DGS
1	1	—	PCB, 1.6 In × 1.255 In × 0.062 In		Any	SLVP234
2	2	—	Shunt, 100 mil, black	0.100	3M	929950–00

3.2 PCB Layout of the TPS62050EVM and TPS62052EVM

The figures below show the layout for the adjustable and fixed output voltage EVMs.

Figure 3–2. Component Placement

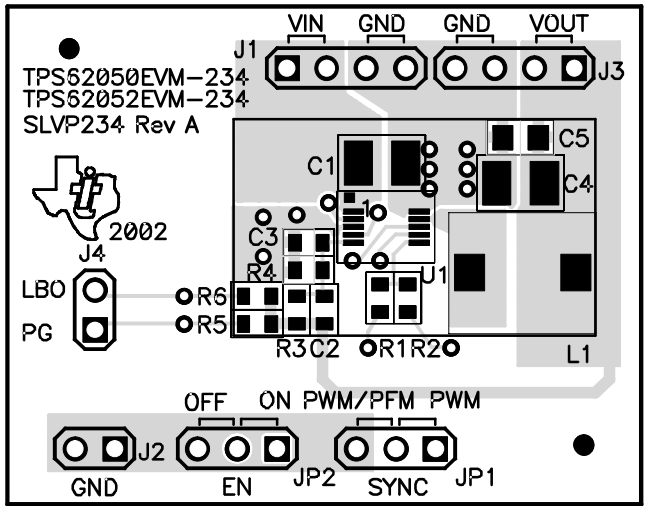

Figure 3–3. Top Layer

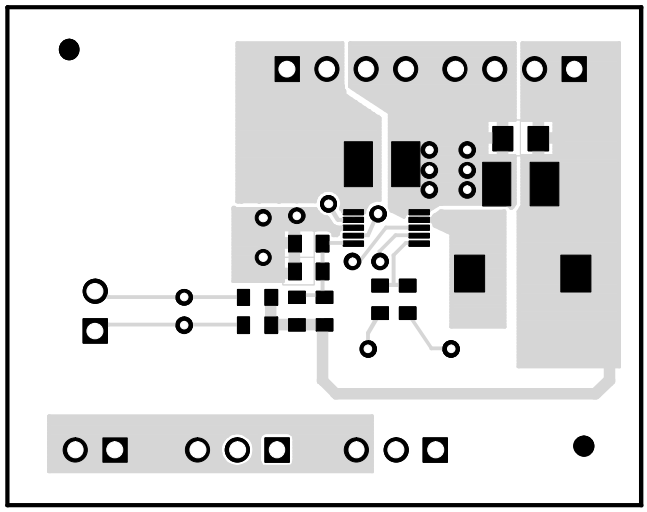

Figure 3–4. Bottom Layer